WHAT IS CLAIMED IS:

1. A semiconductor package device comprising:

a semiconductor chip including a plurality of bonding pads having a microscopic size and aligned at a minute interval;

a planar layer formed on the semiconductor chip so as to expose the bonding pads;

metal patterns formed on the planar layer and having a size larger than a size of the bonding pads in such a manner that at least some parts of the metal patterns are connected to the bonding pads; and

a seed metal layer interposed between the planar layer and the metal patterns.

2. The semiconductor package device as claimed in claim 1, wherein an oxide layer is interposed between the planar layer and the seed metal layer in order to release stress applied thereto.

3. The semiconductor package device as claimed in claim 1, wherein a total thickness of the metal patterns and the seed metal layer is about 1 to 10㎛.

4. The semiconductor package device as claimed in claim 1, wherein the seed metal layer has a triple stack structure including Ti-NiV-CU layers.

5. The semiconductor package device as claimed in claim 1, wherein the bonding pads have a size of 10x10μm in width and length.

6. The semiconductor package device as claimed in claim 1, wherein the metal patterns include an Al-Ag alloy or a Cu-Ag alloy.

7. The semiconductor package device as claimed in claim 1, wherein the metal patterns are aligned in left and right directions or upward and downward directions about the bonding pads.

8. The semiconductor package device as claimed in claim 1, wherein the metal patterns are alternately aligned one by one in a zigzag manner in left and right directions or upward and downward directions about the bonding pads.

9. The semiconductor package device as claimed in claim 9, wherein the metal patterns are inclined with a

predetermined angle.

10. A semiconductor package device comprising:

a semiconductor chip including a plurality of bonding pads having a microscopic size and aligned at a minute interval;

a planar layer formed on the semiconductor chip and having an opening for exposing the bonding pads;

a seed metal layer and metal patterns sequentially formed on the planar layer and having a size larger than a size of the bonding pads in such a manner that at least some parts of the seed metal layer and metal patterns are connected to the bonding pads, the seed metal layer and metal patterns being aligned in left and right directions or upward and downward directions about the bonding pads; and

an oxide layer interposed between the planar layer and the seed metal layer in order to release stress applied thereto.

11. The semiconductor package device as claimed in claim 10, wherein the metal patterns include an Al-Ag alloy or a Cu-Ag alloy.

12. The semiconductor package device as claimed in claim

10, wherein the seed metal layer has a triple stack structure including Ti-NiV-CU layers.

13. A semiconductor package device comprising:

a semiconductor chip including a plurality of bonding pads having a microscopic size and aligned at a minute interval;

a planar layer formed on the semiconductor chip and having an opening for exposing the bonding pads;

a seed metal layer and metal patterns sequentially formed on the planar layer and having a size larger than a size of the bonding pads in such a manner that at least some parts of the seed metal layer and metal patterns are connected to the bonding pads, the seed metal layer and metal patterns being alternately aligned one by one in a zigzag manner in left and right directions or upward and downward directions about the bonding pads; and

an oxide layer interposed between the planar layer and the seed metal layer in order to release stress applied thereto.

14. The semiconductor package device as claimed in claim 13, wherein the seed metal layer and metal patterns are alternately aligned while forming a slightly inclined angle.

15. A method for fabricating a semiconductor package device, the method comprising the steps of:

providing a semiconductor chip including a plurality of bonding pads having a microscopic size and aligned at a minute interval;

forming a planar layer on the semiconductor chip to expose the bonding pads;

forming a seed metal layer on an entire surface of a substrate having the planar layer;

forming solder resist patterns on the seed metal layer such that at least some parts of the solder resist pattern exposes the bonding pads;

forming metal patterns for exposing the solder resist pattern while filling a gap formed between the solder resist patterns;

removing the solder resist patterns; and

etching the seed metal layer by using the metal pattern as a mask.

16. The method as claimed in claim 15, further comprising a step of interposing an oxide layer between the planar layer and the seed metal layer to release stress applied thereto.

17. The method as claimed in claim 15, wherein the solder resist patterns are formed to be thicker than the metal patterns by 1 to 1.7 times.

18. The method as claimed in claim 15, wherein the seed metal layer is formed by sequentially stacking Ti, NiV and Cu layers.